

ABSTRACT

MEMORY ARRAY

A memory array has a multiplicity of row conductors and a multiplicity of column
5 conductors, the row conductors and column conductors being arranged to cross
at cross-points, and has a memory cell disposed at each cross-point, each
memory cell having a storage element and a control element coupled in series
between a row conductor and a column conductor, and each control element
including a silicon-rich insulator. Methods for fabricating the memory array are
10 disclosed.